

## Refine Search

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| L10 and L1 | 1         |

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|                                              | <i>DB=USPT; PLUR=YES; OP=ADJ</i>                                                                             |                            |                                         |
| <u>L12</u>                                   | l10 and l1                                                                                                   | 1                          | <u>L12</u>                              |
| <u>L11</u>                                   | l10 and l4                                                                                                   | 3                          | <u>L11</u>                              |
| <u>L10</u>                                   | L9 and ((micro\$ near4 second\$) or (micro-second\$))                                                        | 790                        | <u>L10</u>                              |
| <u>L9</u>                                    | (timer\$ near4 (generat\$ Or creat\$ or develop\$ or implement\$))                                           | 18696                      | <u>L9</u>                               |
| <u>L8</u>                                    | L7 and (optimiz\$ or overhead\$) near4 (processor\$)                                                         | 27                         | <u>L8</u>                               |
| <u>L7</u>                                    | L6 and (implement\$ Or creat\$ or generat\$ or develop\$) near4 tim\$                                        | 137                        | <u>L7</u>                               |
| <u>L6</u>                                    | l1 and l4                                                                                                    | 186                        | <u>L6</u>                               |
| <u>L5</u>                                    | L4 and l3                                                                                                    | 15                         | <u>L5</u>                               |
| <u>L4</u>                                    | 718/100,101,102,103,104,107.ccls.                                                                            | 3269                       | <u>L4</u>                               |
| <u>L3</u>                                    | L2 and (optimiz\$ or overhead\$) near4 (processor\$)                                                         | 36                         | <u>L3</u>                               |
| <u>L2</u>                                    | L1 and (entry\$ and exit\$)                                                                                  | 223                        | <u>L2</u>                               |
| <u>L1</u>                                    | (schedul\$ near5 thread\$) and (implement\$ Or determin\$ Or develop\$ or creat\$ or maintain\$) near5 tim\$ | 666                        | <u>L1</u>                               |